REMARKS

The Applicant hereby traverses the rejections of record and requests reconsideration and withdrawal of such in view of the remarks contained herein. Claims 1-20 are pending in this application. Claims 1, 8, and 15 have been amended. No new matter has been entered.

Rejection Under 35 U.S.C. § 102(b)

Claims 1, 5, 7, 8, 12, 14, 15, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,905,188 to Chuang et al (hereinafter "Chuang").

It is well settled that to anticipate a claim, the reference must teach every element of the claim. *see* M.P.E.P. § 2131. Moreover, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he elements must be arranged as required by the claim." *see* M.P.E.P. § 2131, citing *In re Bond*, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). Furthermore, in order for a prior art reference to be anticipatory under 35 U.S.C. § 102, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." *see* M.P.E.P. § 2131; *citing Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989).

Claim 1 recites

> a cache memory for storing cache lines in a plurality of memory banks that have a block size that is greater than said memory access size, said cache memory including mapping logic for storing contiguous groups of bits, of size equal to said memory access size, in different ones of said plurality of memory banks.

In the Current Action the Examiner points to Chuang, at Fig. 4 and col. 4 line 57- col. 5 line 56, as teaching this limitation. At the Examiner's citation Chuang merely describes Latin Square Mapping for providing the proper distribution of words on the chip units. This mapping provides that "contiguous words on any given block are stored at different addresses on each chip unit." (*see* Chuang col. 5, lines 20-27). However, Chuang makes no reference to memory banks that have a block size that is greater than said memory access size as recited in claim 1. Furthermore, reference to Fig. 4 makes clear that Chuang does not satisfy this limitation. Rather, Fig. 4 of Chuang shows a series of single blocks where each block corresponds to a single word. Each memory block contained in a 4 block-wide row

communicates with a 4 word ring shift aligner. It necessarily follows that Chuang contemplates only a memory block equal to the memory access size. (*see* Chuang, Fig. 4). Therefore, Chuang fails to teach a plurality of memory banks that have a block size that is greater than said memory access size. Thus, the Applicant requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection of record.

Claim 8 recites

> storing cache lines in memory banks of cache memory included in said processor, said memory banks having a block size that is greater than said memory access size, wherein said storing causes contiguous groups of bits, of size equal to said memory access size, to be stored in different ones of said memory banks;

and claim 15 recites

> a cache memory means for storing cache lines in memory banks according to a block size that is greater than said memory access size, wherein said cache memory means stores contiguous groups of bits, of size equal to said memory access size, in different ones of said plurality of memory banks.

For the reasons set forth above with respect to claim 1, Chuang does not describe at least these limitations in claims 8 and 15. As Chuang does not describe each and every limitation of claims 8 and 15, the Examiner's rejection under 35 U.S.C. § 102(b) is improper and should be withdrawn.

Claims 5 and 7, 12 and 14, and 19-20 depend from claims 1, 8, and 15 respectively, and inherit each limitation of the claim from which they depend. As such, claims 5, 7, 12, 14, 19, and 20 set forth limitations not taught or suggested by the Examiner's proposed combination. Therefore, claims 5, 7, 12, 14, 19, and 20 are patentable at least for the reasons set forth above with respect to claims 1, 8, and 15. Thus, the Applicant requests reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection of record.

Rejection Under 35 U.S.C. § 103(a); Chuang

Claims 6 and 13 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Chuang.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *see* M.P.E.P. § 2143. Without admitting that the first or second criteria are satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the third criteria.

Claims 6 and 13 depend from claims 1 and 8, respectively, and therefore inherit each limitation of the claims from which they depend. As claims 1 and 8 are allowable for at least the reasons set forth above, claims 6 and 13 are allowable as being dependent from an allowable claim.

Rejection Under 35 U.S.C. § 103(a); Middleton

Claims 1-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application No. 2003/0149841 to Middleton (hereinafter "Middleton").

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art cited must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. Without admitting that the second criteria is satisfied, the Applicant respectfully asserts that the Examiner's rejection fails to satisfy the first or third criteria.

Failure to Teach or Suggest All Claim Elements

Claim 1 recites a processor comprising an instruction pipeline for executing processor instructions wherein said processor instructions define a memory access size. In the Current Action, the Examiner acknowledges that Middleton "does not specifically disclose the processor instruction pipeline." (*see* Current Action, paragraph 6A). Moreover, the Applicant respectfully submits that Middleton, even if modified according as the Examiner's suggestion, does not teach or suggest each claim limitation. Middleton discloses a peripheral, or off-chip,

cache. However, the Applicant's invention is drawn to a processor comprising a cache. An off chip cache is not the same as a processor comprising a cache; clearly, Middleton does not teach or suggest the on-chip cache of claim 1. As shown, Middleton fails to teach or suggest each claim limitation. Thus, the Applicant requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of record.

Claim 8 recites a method for operating a processor, comprising executing instructions in an instruction pipeline, wherein said instructions define a memory access size. Claim 15 recites a processor, comprising a pipeline means for executing processor instructions wherein said processor instructions define a memory access size. For the reasons set forth above with respect to claim 1, Middleton does not teach or suggest these limitations in claims 8 and 15. As Middleton does not teach or suggest each and every limitation of claims 8 and 15, the Examiner's rejection under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Claims 2-7, 9-14, and 16-20 depend on claims 1, 8, and 15, respectively, and inherit each element therefrom. As such, claims 2-7, 9-14, and 16-20 set forth limitations not taught or suggested by Middleton. Therefore, claims 2-7, 9-14, and 16-20 are patentable at least for the reasons set forth above with respect to claims 1, 8, and 15. The Applicant requests reconsideration and withdrawal of the 35 U.S.C. 103(a) rejection of record.

Lack of Motivation

The Examiner opines that it would have been obvious "that the cache of Middleton can be part of a processor with an instruction pipeline that provides memory access requests to the cache memory." (*see* Current Action, paragraph 6A). As an initial matter, the Applicant respectfully points out that the Examiner's rejection does not comport with 35 U.S.C. § 103(a) or M.P.E.P. § 2143. The mere fact that a reference can be modified does not render the resultant modification obvious unless the prior art also suggests the desirability of the combination. *see In re Mills*, 916 F.2d 680 (Fed. Cir. 1990); M.P.E.P. § 2143. The Examiner provides a conclusory statement that it would be obvious to modify Middleton as the Examiner proposes, but does not provide any suggestion or motivation for doing so. Nevertheless, the Applicant respectfully points out that modifying the peripheral cache of Middleton to have an instruction pipeline for executing processor instructions would be pointless. A peripheral cache, used for read/write data functions, cannot make any use of an

instruction pipeline executing instructions. Moreover, it would be impossible to place the peripheral cache of Middleton on a processor. As seen at FIG. 5, Middleton requires a cache controller and other memory that stand alone from the cache. Therefore, there would be no suggestion or motivation to modify Middleton as the Examiner proposes. Thus, the Applicant requests reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection of record.

Conclusion

In view of the above remarks, the Applicant believes the pending application is in condition for allowance. The Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 08-2025, under Order No. 200205296-1 from which the undersigned is authorized to draw.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as Express Mail, Airbill No. EV482724137US in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Deposit: January 20, 2006

Typed Name: Laura Horton

Signature: Laura Horton

Respectfully submitted,

By _____
R. Ross Viguet
Reg. No.: 42,203
Date: January 20, 2006
Telephone No. (214) 855-8185